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PATENT

JAN 03 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Hiroshi Miyagi

Application No.: 10/520,510

Filing Date: January 4, 2005

For: SEMICONDUCTOR INTEGRATED CIRCUIT AND SEMICONDUCTOR
INTEGRATED CIRCUIT MANUFACTURING METHOD

Confirmation No.: 5960

Group Art Unit: 2812

Examiner: Not Yet Assigned

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1. Applicant's name	1.
2. Applicant's address	2.
3. Title	3.
4. Filing Date	4.
5. Application Number	5.
6. Foreign/PCT Application Re:	6.
7. Other: Assignment for Published Patent Application	7. Kabushiki Kaisha Toyota Jidoshokki, Aichi-ken, Japan and Niigata Seimitsu Co., Ltd and Niigata-ken, Japan

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Date: January 3, 2006



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Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please mail to the Commissioner for Patents P.O. Box 1450 Alexandria Va 22313-1450. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

Hiroshi Miyagi, Yokohama, JAPAN; ✓

Assignment For Published Patent Application

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Power of Attorney: The patent practitioners associated with Customer Number 23377.

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/JP03/08227 06/27/2003 ✓

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Title

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